

AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 2, 8, 9, 11, 15 and 19 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A liquid crystal display, comprising:
 - a first substrate;
 - a plurality of gate lines formed on the first substrate and transmitting scanning signals;
 - a plurality data lines crossing over the gate lines and transmitting picture signals;
 - a plurality of pixels defined by the gate lines and the data lines, the gate lines diving the pixel electrode into rows and the data lines dividing the pixel electrodes into columns;
 - a protective layer formed over the gate lines and data lines;
 - a plurality of pixel of electrodes formed on the protective layer, each pixel electrode corresponding to one of the plurality of pixels;
 - a second substrate facing the first substrate;
 - a liquid crystal layer formed between said first substrate and said second substrate; and
 - a black matrix defining each pixel; and,
 - wherein: storage capacitance ~~formed~~ is formed between each pixel electrode and the gate line of a previous row, and
 - ~~an opening ratio of the pixels~~ each pixel on a first row has an opening ratio is different from that of ~~the pixels~~ each pixel on the ~~other~~ rest of the rows.

2. (Currently Amended) The liquid crystal display of claim 1, wherein the opening ratio of ~~the pixels~~ each pixel on the first row is smaller than that of each pixel ~~the pixels~~ on the ~~other~~ rest of the rows.

3. (Original) The liquid crystal display of claim 2, wherein the difference in the opening ratio is made by differentiating an opening area of the black matrix.

4. (Previously Presented) The liquid crystal display of claim 3, wherein the black matrix is formed on the second substrate.

5. (Withdrawn) The liquid crystal display of claim 2, wherein the difference in the opening ratio is made through forming a light interception pattern at each pixel of the first pixel row.

6. (Withdrawn) The liquid crystal display of claim 5, wherein the light interception pattern is formed at the same layer as the data line with the same material.

7. (Withdrawn) The liquid crystal display of claim 5, wherein the light interception pattern is formed at the same layer as the gate line with the same material.

8. (Currently Amended) The liquid crystal display of claim 2, wherein the opening ratio of ~~the pixels~~ each pixel on the first row is 60% to 80% of that of ~~the pixels~~ each pixel on the ~~other~~ rest of the rows.

9. (Currently Amended) A liquid crystal display, comprising:

- a first substrate;
- a plurality of gate lines formed on the first substrate and transmitting scanning signals;
- a plurality of data lines crossing over the gate lines and transmitting picture signals;
- a plurality of pixels defined by the gate lines and the data lines, the gate lines dividing the pixels into rows and the data lines dividing the pixels into columns;
- a protective layer formed over the gate lines and the data lines;
- a plurality of pixel electrodes formed on the protective layer, each pixel electrode corresponding to one of the plurality of pixels;
- a second substrate facing the first substrate;
- a liquid crystal layer formed between said first substrate and said second substrate;
- a black matrix defining each pixel; and
- a storage capacitor line formed on said first substrate parallel to the gate line, the storage capacitor line overlapping the pixel electrodes on the first row,

wherein: first storage capacitance is formed between each pixel electrode and the gate line of a previous row, and

second storage capacitance is formed between each pixel electrode on the first row and said storage capacitor line,

a gate-off voltage or a common electrode voltage is applied to said storage capacitor line,

and

~~an opening ratio of each pixel on the first row is~~ has an opening ratio different from that of ~~all the pixels~~ each pixel on the ~~other~~ rest of the rows.

10. (Previously Cancelled)

11. (Currently Amended) The liquid crystal display of claim 9, wherein the opening ratio of ~~the pixels~~ each pixel on the first row is smaller than that of ~~the pixels~~ each pixel on the ~~other~~ rest of the rows.

12. (Original) The liquid crystal display of claim 11, wherein the difference in the opening ratio is made by differentiating an opening area of said black matrix.

13. (Previously Presented) The liquid crystal display of claim 12, wherein said black matrix is formed on said second substrate.

14. (Previously Presented) The liquid crystal display of claim 13, wherein an opening width of said black matrix on the first row is identical to that of said black matrix on the other rows.

15. (Currently Amended) The liquid crystal display of claim 13, wherein an opening length of said black matrix on the first row is smaller than that of said black matrix on the ~~other~~ rest of the rows.

16-18. (Withdrawn)

19. (Currently Amended) The liquid crystal display of claim 11, wherein the opening ratio of ~~the pixels each pixel~~ on the first row is 60% to 80% of that of ~~the pixels each pixel~~ on the ~~other~~ rest of the rows.

20. (Original) The liquid crystal display of claim 9, further comprising a gate-off line formed on said first substrate to transmit a gate-off voltage.

21. (Original) The liquid crystal display of claim 20, wherein the gate-off line and said storage capacitor line are formed at the same layer as the gate line.

22. (Original) The liquid crystal display of claim 21, wherein the gate-off line and said storage capacitor line are electrically connected to each other via a connection member, and the connection member is formed at the same layer as the data line or said pixel electrode.

23. (Previously Presented) The liquid crystal display of claim 9, further comprising:
gate signal transmission films arranged on said first substrate and provided with a gate driving integrated circuit electrically connected to the gate lines for applying gate driving signals thereto; and

data signal transmission films arranged on said first substrate and provided with a data driving integrated circuit electrically connected to the data lines for applying data driving signals thereto,

wherein a common electrode wire for applying the common electrode voltage, a gate-on wire for applying a gate on-voltage to the TFTs controlling the picture signals, a gate-off wire for

applying the gate off-voltage, and wires for transmitting a carry-in signal or a gate-clock signal are extended from an edge portion of the first substrate between the gate signal transmission film and the data signal transmission film.

24. (Original) The liquid crystal display of claim 23, the common electrode wire, the gate-on wire and the gate-off wire are formed at the same layer as the gate lines with the same material.

25. (Withdrawn) A liquid crystal display comprising:
a first insulating substrate;
a plurality of first signal lines formed at the first substrate;
first pads connected to end portions of the first signal lines, the first pads being connected to external driving circuits;
a plurality of second signal lines crossing over the first signal lines while forming pixel areas, the pixel areas collectively forming a display area; and
first light interception patterns positioned outside of the display area, the first light interception patterns being electrically insulated from the first signal lines and the first pads.

26. (Withdrawn) The liquid crystal display of claim 25, wherein the first light interception patterns are not overlapped with the first signal lines and the first pads.

27. (Withdrawn) The liquid crystal display of claim 26, wherein the first light interception patterns are positioned at the region between the display area and the first pads.

28. (Withdrawn) The liquid crystal display of claim 27, wherein the first light interception patterns are spaced apart from the first pads with a predetermined distance.

29. (Withdrawn) The liquid crystal display of claim 25, wherein the first light interception patterns are formed at the same layer as the second signal lines.

30. (Withdrawn) The liquid crystal display of claim 25, further comprising second light interception patterns positioned outside of the display area, the second light interception patterns being electrically insulated from the second signal lines and the second pads.

31. (Withdrawn) The liquid crystal display of claim 30, wherein the second light interception patterns are formed at the same layer as the first signal lines.

32. (Withdrawn) The liquid crystal display of claim 25, further comprising a second insulating substrate facing the first insulating substrate.

33. (Withdrawn) The liquid crystal display of claim 32, further comprising a black matrix defining each pixel area.

34. (Withdrawn) The liquid crystal display of claim 33, wherein the first and second light interception patterns are overlapped with the black matrix.

35. (Withdrawn) The liquid crystal display of claim 32, further comprising a sealer sealing the first and second substrates while surrounding the display area.

36. (Withdrawn) The liquid crystal display of claim 35, wherein the first and second light interception patterns are not overlapped with the sealer.

37. (Withdrawn) The liquid crystal display of claim 32, further comprising color filters formed at the pixel areas.

38. (Withdrawn) The liquid crystal display of claim 32, further comprising a common electrode formed at the second substrate.

39. (Withdrawn) The liquid crystal display of claim 25, further comprising thin film transistors connected to the first and second signal lines, and pixel electrodes positioned at the pixel areas.

40. (Withdrawn) A liquid crystal display comprising:
a first insulating substrate;
a gate line assembly formed at the first insulating substrate, the gate line assembly comprising a plurality of gate lines, gate electrodes branched from the gate lines, and gate pads connected to the gate lines to transmit scanning signals thereto;
first light interception patterns isolated from the gate line assembly;

a gate insulating layer covering the gate line assembly and the first light interception patterns;

a semiconductor layer formed on the gate insulating layer;

a data line assembly formed on the semiconductor layer and the gate insulating layer, the data line assembly comprising a plurality of data lines crossing over the gate lines while forming pixel areas, source electrodes branched from the data lines, drain electrodes positioned opposite to the source electrodes while centering around the gate electrodes, and data pads connected to the data lines to transmit picture signals thereto, the pixel areas collectively forming a display area;

second light interception patterns isolated from the data line assembly;

a protective layer covering the data line assembly and the second light interception patterns, the protective layer having first to third contact holes exposing the gate pad, the data pad and the drain electrode, respectively; and

pixel electrodes connected to the drain electrodes via the third contact holes;

wherein the first and second light interception patterns are positioned outside of the display area.

41. (Withdrawn) The liquid crystal display of claim 40, wherein the first and second light interception patterns are not overlapped with the gate lines and the data lines.

42. (Withdrawn) The liquid crystal display of claim 40, wherein the first and second light interception patterns are spaced apart from the gate pads and the data pads each with a predetermined distance.

43. (Withdrawn) The liquid crystal display of claim 40, further comprising:
a second insulating substrate facing the first substrate;
color filters formed at the second substrate while corresponding to the pixel areas;
a black matrix formed at the second substrate while surrounding the color filters; and
a common electrode covering the color filters and the black matrix.
44. (Withdrawn) The liquid crystal display of claim 43, wherein the first and second light interception patterns are overlapped with the black matrix.
45. (Withdrawn) The liquid crystal display of claim 43, further comprising a sealer sealing the first and second substrates.
46. (Withdrawn) The liquid crystal display of claim 45, wherein the first and second light interception patterns are not overlapped with the sealer.
47. (Withdrawn) The liquid crystal display of claim 40, further comprising an ohmic contact layer formed on the semiconductor layer.
48. (Withdrawn) The liquid crystal display of claim 40, further comprising a subsidiary gate pad covering each gate pad via the first contact hole, and a subsidiary data pads covering each data pad via the second contact hole.

49. (Withdrawn) A method of fabricating a liquid crystal display, the method comprising the steps of:

forming a gate line assembly and first light interception patterns on a first insulating substrate such that the first light interception patterns are separated from the gate line assembly;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly and the first light interception patterns;

forming a semiconductor layer on the gate insulating layer;

forming an ohmic contact layer on the semiconductor layer;

forming a data line assembly and second light interception patterns such that the data line assembly crosses over the gate line assembly while forming pixel areas and the second light interception patterns are separated from the data line assembly, the pixel areas collectively forming a display area, the first and second light interception patterns being positioned outside of the display area;

forming a protective layer such that the protective layer covers the data line assembly and the second light interception patterns; and

forming pixel electrodes on the protective layer.

50. (Withdrawn) The method of claim 49, wherein the first and second light interception patterns are not overlapped with the data line assembly and the gate line assembly.

51. (Withdrawn) The method of claim 49, wherein the semiconductor layer, the ohmic contact layer, the data line assembly, and the second light interception patterns are formed together through one photolithography process.